



174/193

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Paul Metzgen
Application No.: 09/924,272 Confirmation No.: 4896
Filed : August 7, 2001
For : SOFTWARE-TO-HARDWARE COMPILER
Group Art Unit : 2122
Examiner : Not Yet Assigned

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Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

APR 23 2003

Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.56 and 1.97,
applicant wishes to call the attention of the Examiner to
the following documents:

U.S. Patents

| | | |
|--------------|-------------------------|------------|
| Robinson | U.S. Pat. No. 5,068,823 | (11/26/91) |
| Nakai | U.S. Pat. No. 5,142,625 | (08/25/92) |
| Taylor | U.S. Pat. No. 5,535,342 | (07/09/96) |
| Madurawe | U.S. Pat. No. 5,548,228 | (08/20/96) |
| Casselman | U.S. Pat. No. 5,684,980 | (11/04/97) |
| Cooke et al. | U.S. Pat. No. 5,966,534 | (10/12/99) |
| Southgate | U.S. Pat. No. 5,968,161 | (10/19/99) |
| Smith | U.S. Pat. No. 6,085,317 | (07/04/00) |
| Wong et al. | U.S. Pat. No. 6,282,627 | (07/28/01) |

Foreign Patent Documents

European Pat. App. No. EP 0 419 105 A2 (03/27/91)

04/22/2003 TLWU11 00000024 09924272 180.00 DP
01 FC:1806

| | | |
|------------------------|-----------------|------------|
| European Pat. App. No. | EP 0 419 105 A3 | (03/27/91) |
| European Pat. App. No. | EP 0 445 913 A2 | (09/11/91) |
| PCT Pat. App. No. | WO 94/10627 | (05/11/94) |
| European Pat. App. No. | EP 0 759 662 A2 | (02/26/97) |
| PCT Pat. App. No. | WO 97/09930 | (03/20/97) |
| PCT Pat. App. No. | WO 97/13209 | (04/10/97) |
| European Pat. App. No. | EP 0 801 351 A2 | (10/15/97) |
| European Pat. App. No. | EP 0 801 351 A3 | (10/15/97) |
| European Pat. App. No. | EP 0 829 812 A2 | (03/18/98) |
| PCT Pat. App. No. | WO 00/38087 | (06/29/00) |

Other Documents

Callahan, Timothy J. et al. "The Garp Architecture and C Compiler," Computer, April 2000, pp. 62-69.

Cardoso, J M P et al. "Macro-based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Proceedings of Seventh Annual IEEE Symposium, April 21, 1999, Los Alamitos, CA, pp. 2-11.

Edwards, M.D. et al. "Software acceleration using programmable hardware devices," January 1996, pp. 55-63.

ELECTRONIK, DE, FRANZIS VERLAG GMBH - "MIT PROGRAMMIERBARER LOGIK VERHEIRATET," March 31, 1998, Vol. 47, No. 7, p. 38.

Guccione, Steve. List of FPGA-based Computing Machines, <http://www.io.com/~guccione/HW_list.html>, Last Modified March 31, 1999.

IBM, "Programmable Manual Cable Assembly Board," May 1989, IBM Technical Disclosure Bulletin, Vol. 31, pp. 306-309.

Iseli et al. "A C++ compiler for FPGA custom execution synthesis," Proceedings of IEEE Symposium, April 19, 1995, Los Alamitos, CA, pp. 173-179.

Isshiki, T et al. "Bit-serial pipeline synthesis and layout for large-scale configurable systems," Proceedings of The ASP-DAC '97, January 28, 1997, Chiba, Japan, pp. 441-446.

Kastrup, Bernardo et al. "ConCISe: A Compiler-Driven CPLD-Based Instruction Set Accelerator," Proceedings of Seventh Annual IEEE Symposium, April 21, 1999, Los Alamitos, CA, pp. 92-101.

Nanya, T. "Asynchronous VSLI System Design," ASP-DAC '98 Tutorials, February 10, 1998, Yokohama, Japan.

Nanya, T. et al. "Scalable-Delay-Insensitive Design: A high-performance approach to dependable asynchronous systems," Proceedings of International Symposium on Future of Intellectual Integrated Electronics, March, 1999, pp. 531-540.

Page, Ian. "Constructing Hardware-Software Systems from a Single Description," Journal of VSLI Signal Processing, vol. 12, no. 1, January, 1996, pp. 87-107.

Semeria, L. et al. "SpC: synthesis of pointers in C application of pointer analysis to the behavioral synthesis from C," Proceedings of ICCAD International Conference on Computer Aided Design, November 8-12, 1998, San Jose, CA, pp. 340-346.

Wazlowski, M. et al. "PRISM-II compiler and architecture," Proceedings of IEEE Workshop, April 5, 1994, Los Alamitos, CA, pp. 9-16.

Wirthlin, Michael J. et al. "Improving Functional Density Using Run-Time Circuit Reconfiguration," IEEE Transactions on Very Large Scale Integration (VSLI) Systems, Vol. 6, No. 2, June 1998, pp. 247-256.

Wo, D. et al. "Compiling to the gate level for a reconfigurable co-processor," Proceedings of IEEE Workshop, April 10, 1994, Los Alamitos, CA, pp. 147-154.

Copies of the aforementioned documents, which are listed on the accompanying Form PTO-1449 (submitted in duplicate), are enclosed herewith.

Some of the listed documents are being cited because they were recently cited in an International Search Report issued by the European Patent Office in connection with a counterpart International application. A copy of the International Search Report is enclosed herewith.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

A copy of U.S. patent application No. 09/443,971, filed November 19, 1999 is also enclosed herewith. The U.S. patent application document has not been listed on accompanying Form PTO-1449 to prevent its Application No. from being printed on the face of any patent issuing from this application. Applicants respectfully request that the Examiner sign the statement "All references have been considered" at the bottom of the enclosed Form PTO-1449 to indicate that this application was considered (See MPEP § 609) .

Consideration of the foregoing in relation to this
patent application is respectfully requested.

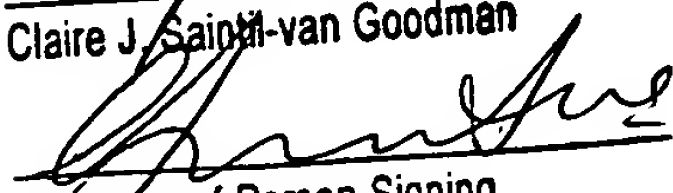
Respectfully submitted,

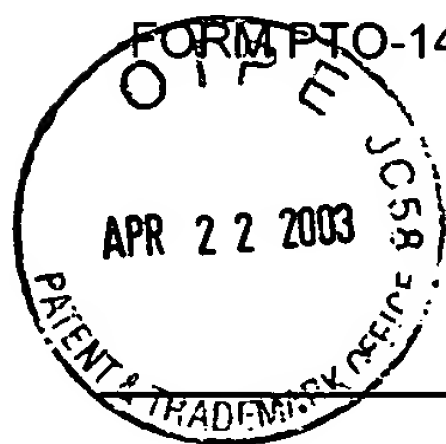


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Claire J. Saintil-van Goodman


Signature of Person Signing



U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

| | |
|-------------------------------|-------------------------------|
| ATTY. DOCKET NO. 174/193 | APPLICATION NO. 09/924,272 |
| APPLICANT Paul Metzgen | CONFIRMATION NO. 4896 |
| FILING DATE August 7, 2001 | GROUP 2122 |

U.S. PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE IF APPROPRIATE |
|---------------------|--------------------|----------|--------------|-------|----------|----------------------------------|
| | 5,068,823 | 11/26/91 | Robinson | 395 | 500 | |
| | 5,142,625 | 08/25/92 | Nakai | 395 | 275 | |
| | 5,535,342 | 07/09/96 | Taylor | 395 | 307 | |
| | 5,548,228 | 08/20/96 | Madurawe | 326 | 41 | |
| | 6,085,317 | 07/04/97 | Smith | 713 | 1 | |
| | 5,684,980 | 11/04/97 | Casselman | 395 | 500 | |
| | 5,966,534 | 10/12/99 | Cooke et al. | 395 | 705 | |
| | 5,968,161 | 10/19/99 | Southgate | 712 | 37 | |
| | 6,085,317 | 07/04/00 | Smith | 713 | 1 | |
| | 6,282,627 | 08/28/01 | Wong et al. | 712 | 15 | |

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FOREIGN PATENT DOCUMENTS

| EXAMINER INITIAL | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
|---------------------|-----------------|----------|---------|-------|----------|-------------|----|
| | | | | | | YES | NO |
| | EP 0 419 105 A2 | 03/27/91 | EPO | G06F | 15/78 | | |
| | EP 0 419 105 A3 | 03/27/91 | EPO | G06F | 15/78 | | |
| | EP 0 445 913 A2 | 09/11/91 | EPO | G06F | 15/60 | | |
| | WO 94/10627 | 05/11/94 | PCT | G06F | 5/00 | | |
| | EP 0 759 662 A2 | 02/26/97 | EPO | H03K | 19/177 | | |
| | WO 97/09930 | 03/20/97 | PCT | A61B | 8/00 | | |
| | WO 97/13209 | 04/10/97 | PCT | G06F | 17/50 | | |
| | EP 0 801 351 A2 | 10/15/97 | EPO | G06F | 13/12 | | |
| | EP 0 801 351 A3 | 10/15/97 | EPO | G06F | 13/12 | | |
| | EP 0 829 812 A2 | 03/18/98 | EPO | G06F | 17/50 | | |
| | WO 00/38087 | 06/29/00 | PCT | G06F | 17/50 | | |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

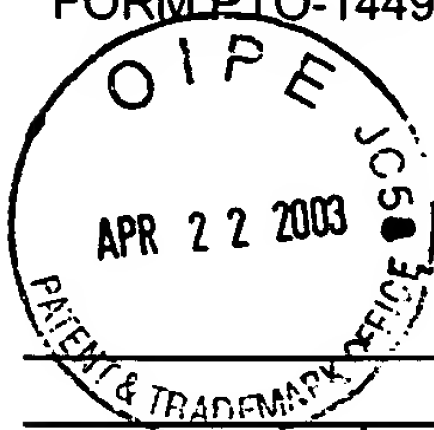
| EXAMINER INITIAL | |
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| | Callahan, Timothy J. et al. "The Garp Architecture and C Compiler," Computer, April 2000, pp. 62-69. |
| | Cardoso, J M P et al. "Macro-based Hardware Compilation of Java™ Bytecodes into a Dynamic Reconfigurable Computing System," Proceedings of Seventh Annual IEEE Symposium, April 21, 1999, Los Alamitos, CA, pp. 2-11. |

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.
174/193APPLICATION NO.
09/924,272APPLICANT
Paul MetzgenCONFIRMATION NO.
4896FILING DATE
August 7, 2001GROUP
2122INFORMATION DISCLOSURE
STATEMENT BY APPLICANT

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER
INITIAL

Edwards, M.D. et al. "Software acceleration using programmable hardware devices," January 1996, pp. 55-63.

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Workshop, April 10, 1994, Los Alamitos, CA, pp. 147-154.**RECEIVED**

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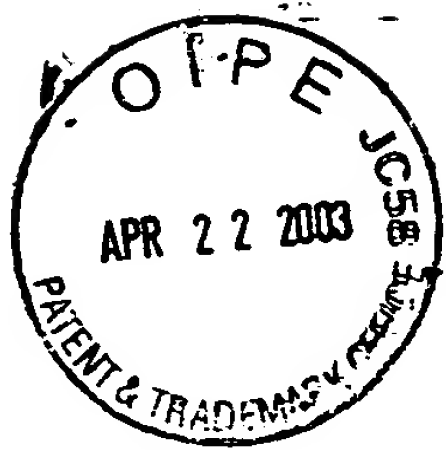
All references have been considered

Examiner

EXAMINER

DATE CONSIDERED

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Rev. 04/01

174/193

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Paul Metzgen
Application No.: 09/924,272 Confirmation No.: 4896
Filed : August 7, 2001
For : SOFTWARE-TO-HARDWARE COMPILER
Group Art Unit : 2122
Examiner : Not Yet Assigned

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Technology Center 2100

New York, New York
April 17, 2003

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TRANSMITTAL LETTER FOR
INFORMATION DISCLOSURE STATEMENT

Sir:

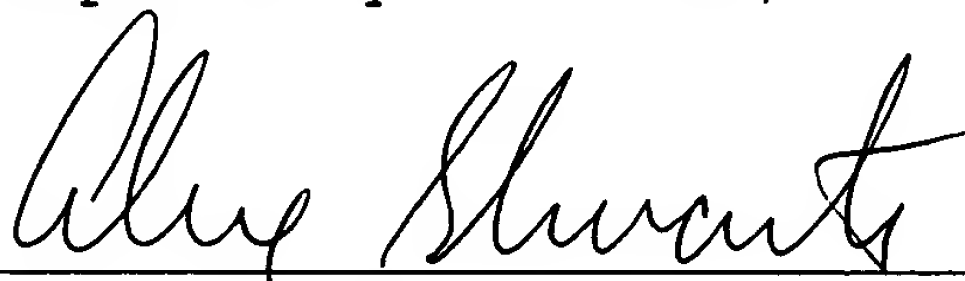
Transmitted herewith is an Information Disclosure Statement and an accompanying Form PTO-1449 (submitted in duplicate) for the above-identified application. This Statement is submitted more than three months from the application filing date, but before the mailing date of the first Office Action on the merits.

Several of the references cited in the Information Disclosure Statement were cited in a communication from a foreign patent office in a counterpart foreign application more than three months prior to the filing of this Statement. In particular, these references were cited in the January 9, 2003 International Search Report in applicant's corresponding Patent Cooperation Treaty Application PCT/US01/41624. A copy of that search report is enclosed herewith.

In accordance with 37 C.F.R. § 1.97, the Information Disclosure Statement is accompanied by a check in the amount of \$180.00 in payment of the fee as set forth in 37 C.F.R. § 1.17(p).

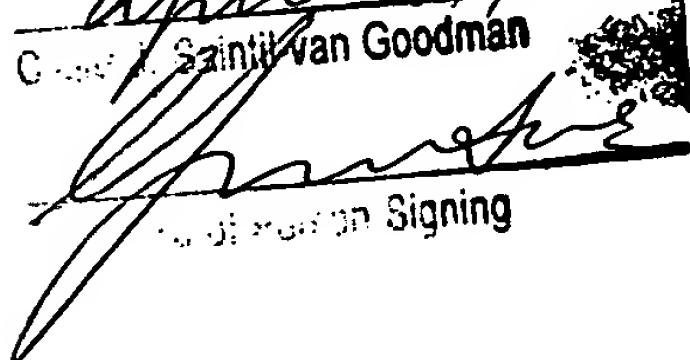
The Director is hereby authorized to charge payment of any additional fees required in connection with the accompanying Information Disclosure Statement, or credit any overpayment, to Deposit Account No. 06-1075. A duplicate copy of this letter is transmitted herewith.

Respectfully submitted,



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April 17, 2003
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